UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,824	08/01/2003	Xavier Montagne	003921.00143	1708

22907 7590 07/13/2009

BANNER & WITCOFF, LTD.
1100 13th STREET, N.W.
SUITE 1200
WASHINGTON, DC 20005-4051

EXAMINER	
TABLER, MATTHEW C	
ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
07/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Arguments

Applicant's arguments filed July 1st, 2009 have been fully considered but they are not persuasive.

The applicant argues that the New et al. reference fails to show "the data processing portion is configured to extract a set of bits from the configuration bit look-up table to map a common plurality of inputs of the reconfigurable interconnect portion to a *plurality of outputs* of the reconfigurable interconnect portion." More specifically, the applicant argues that the prior art fails to show a reconfigurable interconnect portion that maps a *plurality* of inputs to a *plurality* of outputs.

The examiner respectfully disagrees because New et al. show "the data processing portion (330) is configured to extract a set of bits from the configuration bit look-up table (335, 337) to map a common plurality of inputs of the reconfigurable interconnect portion (inputs of 320A-H) to a plurality of outputs of the reconfigurable interconnect portion (110A-H outputs)." The examiner understands that Figure 3 as shown by Lee et al. only illustrates one output and not a plurality of them. The specification however describes a plurality of outputs that are not shown in Figure 3 for simplicity. More specifically, Lee et al. describe a plurality of outputs from the remaining seven MUXs (not shown) connected to the remaining seven input terminals 110B-H in Column 4, lines 7-16. With this in mind, the reconfigurable interconnect portion disclosed by Lee et al. maps a plurality of inputs to a plurality of outputs.

For this reason, claims 1-15 and 35-36 remain rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW C. TABLER whose telephone number is (571)270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. C. T./
Examiner, Art Unit 2819
July 10, 2009

/Vibol Tan/
Primary Examiner, Art Unit 2819